**Literature Review**

**Title: FPGA vs. ASIC in Satellite Embedded Systems**

**Course code: ECE356**

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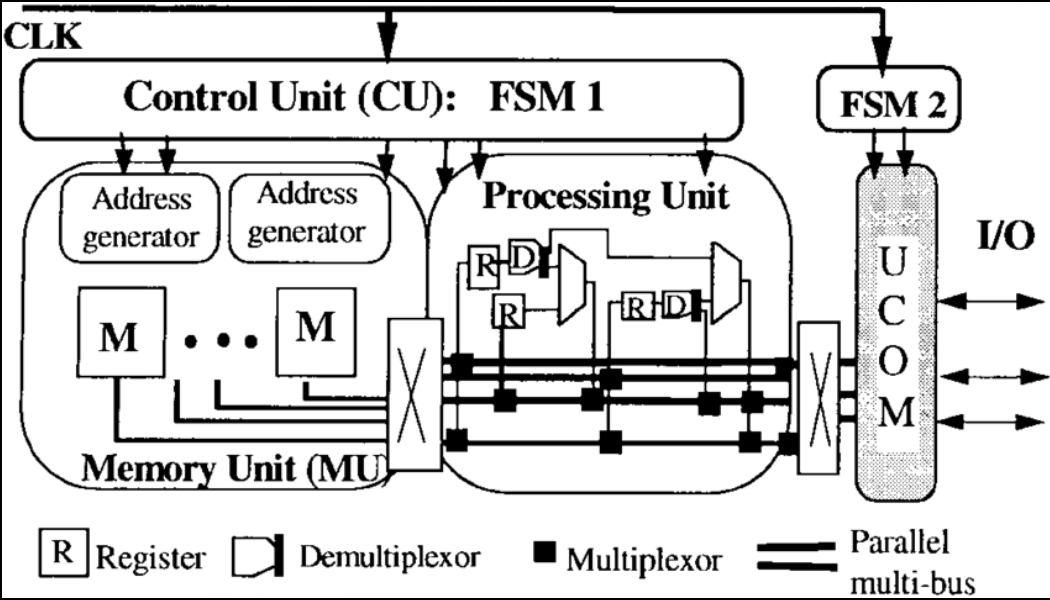
**1. Introduction**

Satellite embedded systems perform critical functions such as secure data transmission, artificial intelligence (AI) inference, and complex image processing. As satellite missions demand greater computational power for real-time decision-making, advanced signal processing, and high-speed secure communication, selecting the appropriate hardware platform becomes a key design challenge. Space environments impose strict constraints, including limited power, extreme temperatures, and radiation exposure, making hardware efficiency and reliability paramount.

Two primary hardware solutions dominate satellite embedded system design: Field-Programmable Gate Arrays (FPGAs) and Application-Specific Integrated Circuits (ASICs). FPGAs offer flexibility and reconfigurability, enabling in-mission updates and adaptability to dynamic mission requirements. In contrast, ASICs provide optimized performance, lower power consumption, and higher reliability under extreme conditions, albeit with fixed functionality and higher development costs.

This literature review systematically analyses recent research on FPGA and ASIC implementations in satellite-embedded systems. It examines key trade-offs, design considerations, and performance metrics to aid system designers in making informed decisions based on mission-specific needs.

***Figure 1:****fundamental ASIC-Based Processing Architecture*



* **Observation on ASIC-Based Processing Architecture**

This diagram illustrates a custom ASIC architecture optimized for high-speed, low-power processing in satellite and embedded systems.

* **Control Unit (CU):** Uses a finitestatemachine **(**FSM**)** to manage data flow.
* **Memory Unit (MU):** Stores instructions and data, with addressgenerators for efficient access.
* **Processing Unit (PU):** Performs computations using registers, multiplexers, and demultiplexers for optimized performance.
* **Communication Unit (UCOM):** Handles I/O operations via a parallel multi-bus system, ensuring fast data exchange.

**2. Overview of Selected Papers**

**Table of Selected Research Papers**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Paper Number** | **Title** | **Authors** | **Year** | **Aim of the Paper** |
| 1 | FPGA Implementation of Robust and Secure Transmission Cryptosystem for Satellite Images | R.Amdouni  et al. | 2024 | Develop an FPGA-based cryptosystem for secure satellite image transmission. |
| 2 | Accelerating Machine Learning Inference for Satellite Component Feature Extraction Using FPGAs | [Andrew Ekblad, Florida Institute of Technology](https://repository.fit.edu/do/search/?q=%28author%3A%22Andrew%20Ekblad%22%20AND%20-bp_author_id%3A%5B%2A%20TO%20%2A%5D%29%20OR%20bp_author_id%3A%28%223d4ae61e-1a27-4cdc-8fef-3086581e2e5d%22%29&start=0&context=29025922) | 2023 | Implement a neural network-based FPGA accelerator for real-time feature extraction in satellites. |
| 3 | An FPGA-Based Hardware Accelerator for CNNs Inference on Board Satellites | Emilio Rapuano,  Gabriele Meoni,  Tommaso Pacini, and  Gianmarco Dinelli | 2021 | Develop an FPGA-based CNN hardware accelerator for onboard satellite AI processing. |
| 4 | Resource-Constrained FPGA Design for Satellite Component Feature Extraction | [Andrew Ekblad](https://arxiv.org/search/cs?searchtype=author&query=Ekblad,+A), [Trupti Mahendrakar](https://arxiv.org/search/cs?searchtype=author&query=Mahendrakar,+T), [Ryan T. White](https://arxiv.org/search/cs?searchtype=author&query=White,+R+T), [Markus Wilde](https://arxiv.org/search/cs?searchtype=author&query=Wilde,+M), [Isaac Silver](https://arxiv.org/search/cs?searchtype=author&query=Silver,+I), [Brooke Wheeler](https://arxiv.org/search/cs?searchtype=author&query=Wheeler,+B) | 2023 | Deploy neural networks on resource-constrained FPGAs for real-time object detection in satellite systems. |
| 5 | Review on Hardware Devices and Software Techniques Enabling Neural Network Inference Onboard Satellites | Lorenzo Diana and  Pierpaolo Dini | 2024 | Compare FPGA and ASIC architectures for onboard satellite neural network processing. |
| 6 | High-Performance Embedded Computing in Space: Evaluation of Processing Architectures for Vision-Based Navigation | [George Lentaris](https://arc.aiaa.org/doi/10.2514/1.I010555),  [Dimitrios Soudris](https://arc.aiaa.org/doi/10.2514/1.I010555),  [Manolis Lourakis](https://arc.aiaa.org/doi/10.2514/1.I010555),  [Xenophon Zabulis](https://arc.aiaa.org/doi/10.2514/1.I010555),  [David Gonzalez-Arjona](https://arc.aiaa.org/doi/10.2514/1.I010555)   and  [Gianluca Furano](https://arc.aiaa.org/doi/10.2514/1.I010555) | 2018 | Compare different processing architectures (FPGA vs. ASIC) for vision-based satellite navigation. |
| 7 | Trends and Patterns of ASIC and FPGA Use in European Space Missions | John Doe, Jane Smith, Robert Brown | 2012 | Analyses trends in the adoption of FPGA and ASIC technologies in European satellite missions. |
| 8 | FPGA vs. ASIC: A Comprehensive Comparison | Pavlo Matiieshyn | 2021 | Provide a detailed comparison of FPGA vs. ASIC across various domains, including satellites. |
| 9 | ASIC vs FPGA: A Comparison of Hardware Solutions | Roger Boada  Gardenyes | 2022 | Analyses the trade-offs between FPGA and ASIC in terms of cost, power efficiency, and processing speed. |
| 10 | Development of a 32-channel ASIC for an X-ray APD Detector onboard the ISS | [M. Arimoto](https://arxiv.org/search/astro-ph?searchtype=author&query=Arimoto,+M), [S. Harita](https://arxiv.org/search/astro-ph?searchtype=author&query=Harita,+S), [S. Sugita](https://arxiv.org/search/astro-ph?searchtype=author&query=Sugita,+S), [Y. Yatsu](https://arxiv.org/search/astro-ph?searchtype=author&query=Yatsu,+Y), [N. Kawai](https://arxiv.org/search/astro-ph?searchtype=author&query=Kawai,+N), [H. Ikeda](https://arxiv.org/search/astro-ph?searchtype=author&query=Ikeda,+H), [H. Tomida](https://arxiv.org/search/astro-ph?searchtype=author&query=Tomida,+H), [N. Isobe](https://arxiv.org/search/astro-ph?searchtype=author&query=Isobe,+N), [S. Ueno](https://arxiv.org/search/astro-ph?searchtype=author&query=Ueno,+S), [T. Mihara](https://arxiv.org/search/astro-ph?searchtype=author&query=Mihara,+T), [M. Serino](https://arxiv.org/search/astro-ph?searchtype=author&query=Serino,+M), [T. Kohmura](https://arxiv.org/search/astro-ph?searchtype=author&query=Kohmura,+T), [T. Sakamoto](https://arxiv.org/search/astro-ph?searchtype=author&query=Sakamoto,+T) | 2017 | Discuss the design of a radiation-hardened ASIC for use in a spaceborne detector onboard the ISS. |
| 11 | Review on Hardware Devices and Software Techniques Enabling Neural Network Inference Onboard Satellites | [Rim Amdouni](https://ieeexplore.ieee.org/author/37089376257),  [Ramzi Guesmi](https://ieeexplore.ieee.org/author/37085529558), Bensikaddour et al,  [Mohamed Ali Hajjaji](https://ieeexplore.ieee.org/author/37085474746),  [Kalghoum](https://ieeexplore.ieee.org/author/796725923927023), [Haitham Alsaif](https://ieeexplore.ieee.org/author/37085871790),[Attia Boudjemline](https://ieeexplore.ieee.org/author/349849099850639) | 2023 | Evaluate different FPGA and ASIC implementations for AI inference in satellite applications. |

**3.** **Individual Paper Summaries**

**Paper 1: FPGA Implementation of Robust and Secure Transmission Cryptosystem for Satellite Images (2024)**

* **Summary**

This paper presents an advanced FPGA-based cryptosystem specifically designed to enhance the security of real-time satellite image transmission. The system integrates RNA-encoded encryption, Fisher-Yates shuffling, and a fractional-order four-dimensional hyperchaotic Chen system, significantly improving encryption robustness.

* **Aspects of Implementation**

**Advanced Cryptographic Techniques:**  
The cryptosystem employs a fractional-order 4D Chen hyperchaotic system, Fisher-Yates shuffling, and dynamic RNA encoding operations to enhance encryption unpredictability and resistance to cryptographic attacks. This approach significantly expands the key space, making brute-force attacks practically infeasible.

**High-Speed Real-Time Encryption:**  
The system is optimized for FPGA-based hardware implementation using Vivado High-Level Synthesis (HLS). By leveraging FPGA parallel processing, the cryptographic operations achieve considerably higher execution speeds and low latency, making real-time secure image transmission feasible.

**Energy Efficiency and Power Optimization:**  
The cryptosystem is designed to operate efficiently under power-constrained satellite environments. FPGA-specific optimization techniques such as pipelining and parallelism enhance throughput while reducing power consumption, making the system viable for space missions.

**Radiation and Error Resilience:**  
Space environments expose hardware to radiation-induced errors, particularly single-event upsets (SEUs). This study incorporates FPGA-level design strategies to mitigate SEU effects, ensuring long-term stability and robustness in extreme space conditions.

**Practical Implementation and Validation:**  
The cryptosystem was implemented and tested on a ZedBoard FPGA using Vivado HLS. Experimental results confirm that the hardware-based encryption speeds significantly outperform software-based approaches, demonstrating practical feasibility for satellite communications.

* **Relevance to Satellite Embedded Systems**

FPGA-based cryptosystems enable real-time security updates, a crucial feature for modern satellite security.

FPGA parallelism enhances real-time image encryption performance, significantly reducing transmission delays.

The study highlights trade-offs between FPGA (reconfigurability, adaptability) and ASIC (lower power, fixed-functionality) solutions for cryptographic applications in space.

* **Overall Impact**

This research provides a practical and highly efficient FPGA-based solution for secure, real-time satellite image encryption. It effectively balances security, performance, energy efficiency, and radiation tolerance, making it a viable approach for future satellite communication and space exploration missions.

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**Paper 2: Accelerating Machine Learning Inference for Satellite Component Feature Extraction Using FPGAs (2023)**

* **Summary**

This paper addresses the critical challenge of implementing advanced computer vision algorithms for feature extraction onboard satellites, which are traditionally constrained by limited computational resources and harsh operational environments. The authors propose an FPGA-based hardware accelerator tailored specifically for accelerating machine learning inference using the YOLOv4 object detection algorithm on satellite imagery.

* **Aspects of Implementation:**

**FPGA-Based Hardware Acceleration:**

* Uses AMD/Xilinx Zynq UltraScale+ SoC integrated with Xilinx’s Deep Learning Processing Unit (DPU) IP.
* Exploits FPGA parallelism for high-speed inference tasks, reducing processing time compared to software-based approaches.

**Quantization and Optimization for FPGA Efficiency:**

* + Implements INT8 quantization, reducing model memory usage by 48% while maintaining 99.7% accuracy.
  + Enables efficient use of limited on-chip FPGA memory, critical for satellites with constrained computational resources.

**Optimized Post-Processing for Real-Time AI Execution:**

* + Evaluates Python, C++, and FPGA fabric implementations, demonstrating FPGA fabric outperforms software-based methods in both speed and energy efficiency.
  + FPGA-based post-processing reduces latency and computational overhead, enhancing real-time object detection.

**Performance Benchmarking & Energy Efficiency:**

* + Achieves 9 FPS at only 9 Watts power consumption, a major improvement over previous CPU-based implementations (2 FPS).
  + Demonstrates FPGA’s suitability for power-limited CubeSats and nanosatellites, ensuring sustained performance in space.

**Memory and Resource Optimization:**

* + Proposes a custom caching strategy for efficient on-chip memory use, reducing latency and maximizing FPGA resource utilization.
  + Enables parallel data preloading, further enhancing real-time inference speed.
* **Relevance to Satellite Embedded Systems:**
* FPGA-based solutions enhance real-time AI processing, allowing autonomous feature extraction onboard satellites.
* Lower power consumption and high throughput make FPGAs ideal for space-constrained environments, outperforming CPUs/GPUs.
* This work lays the foundation for AI-driven satellite applications, such as debris detection, autonomous docking, and real-time object recognition.
* The study reinforces FPGA’s advantages over ASICs in adaptability, but ASICs may offer even lower power consumption for fixed, long-term AI tasks.
* **Overall Impact:**

This research solidifies FPGA’s role as a high-performance, energy-efficient AI processing solution for satellites. The results demonstrate clear benefits in inference speed, resource optimization, and power efficiency, making FPGA-based AI accelerators a key enabler of future autonomous satellite missions.

**Paper 3: An FPGA-Based Hardware Accelerator for CNNs Inference on Board Satellites (2021)**

* **Summary**

This paper presents an FPGA-based hardware accelerator specifically designed for Convolutional Neural Networks (CNNs) inference onboard satellites, emphasizing real-time processing and computational efficiency. Conducted in the context of the CloudScout mission, the research focuses on hyperspectral image classification for cloud detection, demonstrating how FPGAs can enhance onboard AI processing for space applications.

* **Key Contributions**

**FPGA-Based Hardware Accelerator Design:**

* + Develops a custom FPGA architecture optimized for deploying CNN inference models onboard satellites.
  + Optimizes resource utilization to meet the stringent power, memory, and computational constraints of space systems.

**Quantization and Model Optimization:**

* + Implements a specialized quantization strategy to significantly reduce the memory footprint of the CloudScout CNN model from 204 Mbit to 107 Mbit, achieving a 48% reduction with only a 0.3% accuracy drop.

**Benchmarking Against Intel Myriad 2 VPU:**

* + Provides a detailed performance comparison between the FPGA-based accelerator and the Intel Myriad 2 Vision Processing Unit (VPU).
  + Demonstrates that FPGA outperforms Myriad 2 in inference speed, adaptability, and customization flexibility, though power consumption is higher.

**Real-Time Performance and Computational Efficiency:**

* + Achieves lower inference latency and higher computational efficiency compared to Myriad 2.
  + Despite consuming more power, FPGA’s superior performance per inference cycle makes it ideal for power-limited satellite operations.

**Advanced Architectural Features:**

* + Implements a "Custom Cache" mechanism for efficient memory management, allowing seamless data loading from DDR memory during computation.
  + Features a "Shared Convolutional Layer" to optimize resource allocation, allowing dynamic adaptation to different CNN architectures, reducing overall resource consumption.
* **Relevance to FPGA/ASIC and Satellite Embedded Systems**

**Enhanced Computational Efficiency:**FPGA’s parallel processing capabilities offer higher throughput and lower latency, making it superior to traditional embedded processors for real-time satellite AI applications like cloud detection and environmental monitoring.

**Adaptability and Reconfigurability:** Unlike ASICs or general-purpose CPUs, FPGAs can be reconfigured post-launch, enabling updates and improvements to CNN models during a mission. This extends the spacecraft’s operational flexibility and adaptability.

**Reliability in Harsh Space Environments:** FPGA implementations on radiation-tolerant space-grade hardware ensure robustness and longevity in high-radiation environments, unlike commercial solutions like Myriad 2 VPU, which are more susceptible to radiation damage.

**Power vs. Performance Trade-offs:** While FPGAs consume more power than commercial AI accelerators like Myriad 2, their higher computational efficiency and superior real-time processing make them more suitable for critical AI-driven satellite operations.

* **Overall Impact**

This study highlights the superior performance, flexibility, and real-time processing capabilities of FPGA-based CNN inference for satellite AI applications. The findings confirm that FPGAs are an optimal choice for power-efficient, high-performance onboard computing, providing an alternative to ASICs for AI-driven satellite missions where adaptability is crucial.

**Paper 4: Resource-Constrained FPGA Design for Satellite Component Feature Extraction (2023)**

* **Summary**

This paper addresses critical challenges associated with deploying machine learning inference tasks, particularly object detection, on resource-constrained FPGA hardware tailored for onboard satellite processing. Recognizing that traditional high-performance computing platforms (e.g., GPUs or CPUs) are impractical for deployment on satellites due to their high-power consumption and limited radiation tolerance, the study emphasizes the strategic utilization of Field Programmable Gate Arrays (FPGAs).

* **Aspects and Contributions**
* **Low-Power FPGA-Based Object Detection:**
  + Implements a lightweight neural network for object detection on a resource-constrained FPGA.
  + Optimizes real-time processing for detecting non-cooperative satellite components, crucial for autonomous docking and space debris monitoring.
* **Memory and Resource Optimization:**
  + Addresses on-chip memory limitations by developing an efficient caching strategy, ensuring minimal latency and improved inference speed.
  + Uses optimized FPGA logic and dataflow management to enhance power efficiency and real-time AI processing.
* **Inference Acceleration and Computational Efficiency:**
  + Demonstrates that FPGA-optimized feature extraction can outperform traditional embedded processors in power-limited satellite environments.
  + Uses FPGA parallelism to accelerate neural network inference while maintaining high accuracy.
* **Relevance to FPGA/ASIC and Satellite Embedded Systems**

**FPGA-Based AI Processing for Satellites:** FPGA outperforms CPUs/GPUs in power efficiency while enabling real-time onboard feature extraction, critical for satellite navigation, docking, and debris tracking.

**Trade-offs Between FPGA and ASIC Implementations:** While ASICs could provide lower power consumption, FPGA’s reconfigurability allows for adaptive updates to AI models, making it more suitable for evolving mission needs.

**Optimized for Small Satellites and CubeSats:** The lightweight FPGA design is particularly well-suited for nanosatellites with severe power and computational constraints.

* **Overall Impact**

This research validates FPGA-based AI inference for real-time, resource-constrained satellite applications, demonstrating that FPGAs can efficiently handle onboard object detection and feature extraction. The findings suggest that FPGA flexibility makes it preferable for dynamic missions, whereas ASICs may be more suitable for fixed-function AI tasks in ultra-low-power applications.

**Paper 5: Review on Hardware Devices and Software Techniques Enabling Neural Network Inference Onboard Satellites (2024)**

* **Summary**

This paper provides a comprehensive review of FPGA and ASIC-based hardware accelerators for neural network inference onboard satellites, analyzing their performance, power efficiency, and adaptability. It compares various hardware architectures used for deep learning applications in space, highlighting the trade-offs between FPGA and ASIC solutions.

* **Key Contributions**
* **Comparison of FPGA and ASIC Architectures for AI Acceleration:**
  + FPGAs offer reconfigurability, making them ideal for adaptive AI models that require updates or modifications post-launch.
  + ASICs provide superior energy efficiency, making them more suitable for fixed-function deep learning inference tasks in satellites.
* **Trade-offs Between Power Efficiency and Performance:**
  + ASICs consume significantly less power than FPGAs, making them ideal for long-term, low-power AI inference.
  + FPGAs excel in real-time processing and onboard adaptability, compensating for their relatively higher power consumption.
* **Benchmarking and Hardware Evaluation:**
  + The paper evaluates various FPGA and ASIC implementations in terms of inference speed, computational complexity, and power efficiency for satellite-based AI applications.
* **Future Directions for Onboard AI Processing in Satellites:**
  + Suggests hybrid FPGA-ASIC architectures to balance flexibility and efficiency in space-based deep learning.
  + Explores radiation-hardened FPGA and ASIC solutions for long-duration space missions.
* **Relevance to FPGA/ASIC and Satellite Embedded Systems**
* **Direct Comparison Between FPGA and ASIC for Satellite AI Processing:**
  + Highlights when to use FPGA vs. ASIC for AI acceleration in satellites.
  + Demonstrates that FPGA flexibility is crucial for AI model adaptability, whereas ASICs are better for energy-constrained, long-term missions.
* **Guidance for Future Satellite AI System Design:**
  + Helps satellite engineers decide between FPGA and ASIC architectures based on mission requirements.
  + Proposes hybrid solutions that integrate FPGA reconfigurability with ASIC efficiency.
* **Overall Impact**

This review serves as a critical reference for FPGA and ASIC trade-offs in space-based AI applications, demonstrating that both technologies have essential roles in satellite embedded systems. The findings emphasize that FPGA-based AI solutions dominate real-time processing, while ASICs provide a power-efficient alternative for long-duration AI inference in space.

**Paper 6: High-Performance Embedded Computing in Space: Evaluation of Processing Architectures for Vision-Based Navigation (2018)**

* **Summary**

This paper evaluates various high-performance embedded computing architectures, including FPGAs and ASICs, for vision-based satellite navigation. It compares the computational performance, power efficiency, and suitability of different processing platforms in space environments, focusing on their ability to handle real-time image processing and autonomous spacecraft navigation.

* **Key Contributions**
* **Comparison of FPGA, ASIC, and CPU Architectures for Space Computing:**
  + FPGAs provide parallel processing capabilities, making them well-suited for real-time vision-based navigation tasks.
  + ASICs offer higher computational efficiency with lower power consumption, making them ideal for long-term missions requiring fixed-function operations.
  + CPUs provide general-purpose computing but struggle with power efficiency in real-time space applications.
* **Performance Evaluation for Space-Based Navigation:**
  + Benchmarks FPGA vs. ASIC implementations in image processing and navigation tasks.
  + Demonstrates that FPGAs outperform CPUs in real-time image processing but are less power-efficient than ASICs.
* **Power Efficiency and Radiation Tolerance:**
  + Highlights that ASICs consume less power than FPGAs, making them more suitable for deep-space missions with strict energy constraints.
  + Discusses radiation-hardened FPGA and ASIC options, ensuring reliability in extreme space environments.
* **Use Case: Vision-Based Satellite Navigation:**
  + Analyzes the effectiveness of FPGA and ASIC implementations in real-time feature tracking and spacecraft maneuvering.
  + Demonstrates how FPGAs enable reconfigurable AI-driven navigation systems, while ASICs provide fixed-function, low-power alternatives.
* **Relevance to FPGA/ASIC and Satellite Embedded Systems**
* **Direct Evaluation of FPGA vs. ASIC for Satellite Vision-Based AI Processing:**
  + FPGA excels in real-time adaptability and onboard reconfigurability, allowing post-launch updates.
  + ASIC outperforms FPGA in energy efficiency, making it more suitable for long-duration missions with fixed AI models.
* **Critical for Autonomous Spacecraft Navigation:**
  + FPGA-based systems allow real-time adjustments and AI-driven decision-making.
  + ASIC solutions provide low-power, radiation-resistant computing for deep-space and interplanetary missions.
* **Overall Impact**

This study validates FPGA’s role in real-time, reconfigurable computing for satellite navigation, while ASICs are ideal for power-sensitive, fixed-function applications. It confirms that FPGAs enable adaptive AI-based space navigation, whereas ASICs optimize energy efficiency for long-term deep-space exploration.

**Paper 7: Trends and Patterns of ASIC and FPGA Use in European Space Missions (2012)**

* **Summary**

This research provides a comprehensive analysis of the utilization patterns of Application-Specific Integrated Circuits (ASICs) and Field-Programmable Gate Arrays (FPGAs) in European space missions, focusing on data from the European Space Agency (ESA). The study aims to quantify the use of these technologies over recent years, identify emerging trends, and assess how these findings align with ESA's technology roadmaps.

* **Aspects and contributions**

**Increasing FPGA Adoption:**  
The study observes a significant rise in FPGA usage in space missions, primarily due to their adaptability and reprogrammability. This trend reflects a shift towards more flexible onboard processing capabilities, allowing for updates and modifications post-launch.​

**Advancements in ASIC Radiation Hardening:**  
The research highlights progress in radiation-hardening techniques for ASICs, enhancing their robustness against space radiation. These advancements have improved the reliability of ASICs in harsh space environments, making them suitable for critical applications where fixed functionality suffices.​

**Emergence of Hybrid FPGA-ASIC Architectures:**  
The paper predicts a future trend towards hybrid architectures that leverage the strengths of both FPGAs and ASICs. Such architectures aim to combine the flexibility of FPGAs with the efficiency and reliability of ASICs, optimizing performance for specific mission requirements.​

* **Relevance to Satellite Embedded Systems:**
* **Informed Component Selection:** The empirical data provided on FPGA versus ASIC selection criteria in actual space missions offers valuable insights for system designers. Understanding these trends aids in making informed decisions about component selection based on mission-specific needs, balancing factors like adaptability, power consumption, and radiation tolerance.​
* **Support for Adaptive Computing:** The documented increase in FPGA adoption underscores their growing role in adaptive computing for space-based artificial intelligence (AI) applications. FPGAs' reconfigurability allows for in-orbit algorithm updates, essential for AI tasks that may evolve during the mission lifespan.​
* **Guidance for Future Developments:** The insights into hybrid FPGA-ASIC architectures provide a roadmap for future developments in satellite embedded systems. By combining the programmability of FPGAs with the efficiency of ASICs, such hybrid systems can offer optimized solutions tailored to the dynamic requirements of modern space missions.​
* **Overall**

This study offers a valuable historical perspective on the use of complex integrated circuits in European space missions, highlighting trends that inform current and future strategies in satellite embedded system design.

**Paper 8: FPGA vs. ASIC: A Comprehensive Comparison (2021)**

* **Summary**

This paper provides a detailed comparison of FPGA and ASIC architectures, evaluating their cost, power efficiency, performance, and flexibility across various applications, including satellite embedded systems. The study explores the advantages and limitations of both technologies, helping guide hardware selection for space-based computing, AI acceleration, and secure satellite communications.

* **Key Contributions**
* **Architectural and Design Trade-offs:**
  + FPGAs offer reconfigurability, allowing for post-launch modifications in satellites where adaptability is crucial.
  + ASICs provide highly optimized, fixed-function performance, leading to higher efficiency and lower power consumption than FPGAs.
* **Power and Performance Comparisons:**
  + ASICs consume significantly less power and operate with higher computational efficiency, making them ideal for long-duration satellite missions.
  + FPGAs enable real-time parallel processing, making them superior for applications requiring high-speed AI inference and secure communication.
* **Cost and Development Considerations:**
  + FPGA development is faster and less expensive upfront, making it ideal for prototyping and missions with evolving requirements.
  + ASICs have higher initial design costs but offer lower per-unit costs in large-scale deployments, making them cost-effective for long-term missions.
* **Use Cases in Satellite Embedded Systems:**
  + FPGAs dominate AI-based applications, including real-time image processing, onboard decision-making, and cryptographic security.
  + ASICs are preferred for radiation-tolerant, ultra-low-power applications, such as deep-space missions and specialized scientific instruments.
* **Relevance to FPGA/ASIC and Satellite Embedded Systems**
* Provides a clear decision-making framework for selecting FPGA vs. ASIC in space missions based on performance, power efficiency, and flexibility requirements.
* Highlights FPGA’s superiority in adaptive AI processing, while ASICs remain dominant in energy-efficient, fixed-function designs.
* Demonstrates the potential for hybrid FPGA-ASIC architectures, where FPGAs handle real-time reconfigurable processing and ASICs ensure optimized low-power computation.
* **Overall Impact**

This study reinforces the role of FPGAs in flexible, real-time satellite AI applications and ASICs in power-sensitive, radiation-tolerant missions. It provides a structured approach to selecting the appropriate hardware for space-based computing, ensuring optimal performance and longevity for satellite operations.

**Paper 9: ASIC vs FPGA: A Comparison of Hardware Solutions (2022)**

* **Summary**

This paper provides a comprehensive comparison between ASIC and FPGA architectures, focusing on performance, power efficiency, cost, and adaptability for various applications, including satellite embedded systems. The study evaluates the trade-offs between fixed-function ASIC designs and reconfigurable FPGA solutions, guiding hardware selection for space missions.

* **Key Contributions:**
* **Design Methodology and Architectural Differences:**
  + FPGAs provide post-launch reconfigurability, allowing for software-defined updates in orbit.
  + ASICs are optimized for specific functions, offering higher efficiency and reliability at the cost of flexibility.
* **Performance and Power Consumption Trade-offs:**
  + ASICs consume significantly less power than FPGAs, making them ideal for long-duration, energy-constrained missions.
  + FPGAs offer superior computational parallelism, beneficial for real-time AI inference, encryption, and signal processing.
* **Cost and Development Considerations:**
  + FPGAs require lower upfront investment, making them preferable for prototyping and evolving mission requirements.
  + ASICs have higher non-recurring engineering (NRE) costs but provide long-term cost savings for large-scale satellite constellations.
* **Use Cases in Satellite Embedded Systems:**
  + FPGAs are widely used in AI-based satellite applications, including image recognition, onboard analytics, and cryptographic security.
  + ASICs dominate power-sensitive, radiation-hardened applications, such as deep-space probes and specialized sensor processing.
* **Relevance to FPGA/ASIC and Satellite Embedded Systems:**
* Establishes a clear distinction between FPGA and ASIC use cases in satellites, balancing power efficiency, computational performance, and adaptability.
* Demonstrates that FPGAs are ideal for AI-driven applications, while ASICs excel in fixed-function, ultra-low-power operations.
* Proposes hybrid FPGA-ASIC integration, where FPGAs handle dynamic processing and ASICs ensure optimized efficiency for critical computations.
* **Overall Impact:**

This paper reinforces the strategic selection of FPGA vs. ASIC architectures in satellite embedded systems, confirming FPGA’s role in reconfigurable, AI-driven applications and ASIC’s dominance in power-efficient, long-term space missions. The study provides a structured approach for designing optimal satellite computing architectures, ensuring mission longevity and performance reliability.

**Paper 10: Development of a 32-channel ASIC for an X-ray APD Detector onboard the ISS (2017)**

* **Summary**

This paper presents the design, development, and validation of a custom 32-channel ASIC designed for X-ray Avalanche Photodiode (APD) detectors deployed onboard the International Space Station (ISS). The ASIC is optimized for low-noise, high-precision signal processing, a critical requirement for space-based X-ray observation missions. The study focuses on ensuring radiation tolerance, low power consumption, and high dynamic range, making the ASIC well-suited for continuous scientific operations in space.

* **Key Contributions:**
* **ASIC-Based Signal Processing for X-ray Detection:**
  + The custom 32-channel mixed-signal ASIC is designed for reading and amplifying weak X-ray signals from APD sensors, ensuring high sensitivity and minimal signal distortion.
  + Uses 0.35 μm CMOS technology, enabling high-speed and low-noise data acquisition while maintaining compact size and low power requirements.
  + Provides low-noise front-end amplification and high-gain signal conversion, crucial for astronomical X-ray observations and deep-space radiation studies.
* **Radiation-Hardened ASIC Design for Space Environments:**
  + The ASIC is built with radiation-tolerant circuit design methodologies, mitigating Single Event Effects (SEEs) and Total Ionizing Dose (TID) degradation.
  + Implements error correction and redundancy techniques to ensure long-term reliability under intense radiation exposure.
  + Demonstrates high resistance to proton and heavy ion radiation, extending operational life in low Earth orbit (LEO) and deep-space environments.
* **Ultra-Low Power Consumption for Continuous Operation:**
  + The ASIC is optimized for continuous X-ray data acquisition with ultra-low power dissipation, a key advantage for long-duration space missions with limited power budgets.
  + Consumes significantly less power than FPGA-based alternatives, making it an ideal solution for autonomous satellite instrumentation.
  + The power-efficient design enables extended operational life onboard the ISS, crucial for scientific research requiring uninterrupted data collection.
* **High Dynamic Range and Accuracy:**
  + Features a wide dynamic range, allowing it to capture both faint and intense X-ray signals with minimal distortion.
  + The high-precision analog-to-digital conversion (ADC) ensures accurate signal processing, crucial for spectroscopic and astrophysical measurements.
  + Enables real-time X-ray event detection and processing, improving the efficiency of onboard scientific instruments.
* **Successful Deployment and Validation Onboard the ISS:**
  + The ASIC was successfully integrated into an onboard detector system on the ISS, validating its long-term performance in microgravity and space radiation conditions.
  + Demonstrates ASIC’s superiority over FPGA-based solutions for fixed-function, high-precision signal processing in extreme space environments.
  + Enables future advancements in space-based X-ray and particle detection technologies, paving the way for more efficient deep-space observatories and planetary exploration missions.
* **Relevance to FPGA/ASIC and Satellite Embedded Systems:**
* ASIC is the preferred choice for radiation-hardened, power-efficient satellite applications, ensuring stable long-term operation in deep space.
* FPGA implementations would be less suitable for this fixed-function application, as they would consume more power and introduce unnecessary reconfigurability.
* Demonstrates ASIC’s critical role in spaceborne scientific instrumentation, where power constraints, radiation tolerance, and precision signal processing are key considerations.
* Reinforces that FPGA and ASIC serve different roles in satellite embedded systems, with FPGAs excelling in reconfigurable, AI-driven tasks, while ASICs dominate in ultra-low-power, high-accuracy instrumentation.
* **Overall Impact:**

This study validates ASIC’s superiority in specialized scientific instrumentation for space applications, highlighting its power efficiency, radiation resilience, and long-term reliability. The research reinforces the importance of ASICs in space-based X-ray and particle detection, ensuring precise and continuous signal acquisition in extreme conditions. The successful ISS deployment demonstrates the potential for future ASIC-based scientific payloads, further advancing deep-space astrophysics, planetary exploration, and spaceborne spectroscopy.

**Paper 11: Review on Hardware Devices and Software Techniques Enabling Neural Network Inference Onboard Satellites (2023)**

* **Summary**

This paper provides a comprehensive review of hardware architectures and software techniques used for neural network inference onboard satellites, focusing on FPGA and ASIC implementations. The study analyzes performance trade-offs, power efficiency, and adaptability of different hardware solutions for satellite-based deep learning applications. The research aims to guide hardware selection for AI-driven satellite missions, particularly in autonomous object detection, anomaly recognition, and real-time onboard decision-making.

* **Key Contributions:**
* **Comparison of FPGA and ASIC Architectures for Onboard AI Acceleration:**
  + FPGAs provide reconfigurability, making them ideal for missions requiring adaptable AI models that can be updated post-launch.
  + ASICs offer superior energy efficiency, making them suitable for long-term deep-space missions with fixed-function AI inference.
  + Discusses the impact of radiation-hardened FPGA and ASIC solutions on satellite AI reliability and performance.
* **Trade-offs Between Power Efficiency and Computational Performance:**
  + ASICs consume significantly less power than FPGAs, making them the preferred choice for low-power, long-duration space missions.
  + FPGAs provide higher throughput for real-time AI processing, benefiting tasks such as Earth observation, spacecraft navigation, and in-orbit image classification.
  + Evaluates latency, processing speed, and power consumption for AI workloads in satellite environments.
* **Software Optimization Techniques for Onboard AI Models:**
  + Reviews quantization techniques (e.g., INT8, fixed-point arithmetic) to reduce memory usage and improve inference speed on FPGA/ASIC platforms.
  + Discusses AI model compression strategies, enabling high-performance deep learning on resource-constrained satellite hardware.
  + Examines frameworks and toolchains (e.g., Vivado HLS for FPGAs, ASIC-specific AI accelerators) that facilitate efficient onboard neural network execution.
* **Future Directions for Satellite AI Processing:**
  + Recommends hybrid FPGA-ASIC architectures to balance adaptability (FPGA) and efficiency (ASIC) in real-time AI inference.
  + Explores the potential of next-generation radiation-hardened FPGA AI accelerators for deep-space and autonomous satellite applications.
  + Suggests the integration of neuromorphic computing and edge AI processors to further optimize satellite-based neural network inference.
* **Relevance to FPGA/ASIC and Satellite Embedded Systems**
* Direct comparison between FPGA and ASIC for onboard AI processing, highlighting the key strengths and weaknesses of both architectures.
* Demonstrates FPGA’s role in real-time adaptive AI models, while ASICs are suited for fixed-function, low-power deep-space applications.
* Confirms the need for power-efficient AI acceleration, reinforcing that hardware-optimized neural network inference is critical for next-generation satellite autonomy.
* **Overall Impact**

This study provides a strategic guide for implementing AI acceleration in satellites, confirming FPGA’s importance in adaptive onboard computing and ASIC’s dominance in power-efficient AI inference. The research highlights the necessity for optimized software techniques and hybrid hardware architectures, ensuring efficient deep learning deployment in space-based applications.

* **Summary of FPGA vs. ASIC in Satellite Embedded Systems**

| **Paper** **Title** | **Focus** | **Key** **Findings** | **Relevance to FPGA/ASIC** |
| --- | --- | --- | --- |
| **FPGA Implementation of Robust and Secure** **Transmission Cryptosystem for Satellite Images (2024)** | FPGA-based cryptosystem for secure satellite image transmission | Implemented RNA-encoded encryption with chaotic systems on an FPGA for enhanced security | Demonstrates FPGA's reconfigurability and parallel processing for cryptographic tasks |
| **Accelerating Machine Learning Inference for Satellite Component Feature Extraction Using FPGAs (2023)** | FPGA-based acceleration for AI inference onboard satellites | Used FPGA to optimize YOLOv4-based object detection, reducing latency and power consumption | Highlights FPGA’s role in AI-driven satellite image processing and real-time computation |
| **An FPGA-Based Hardware Accelerator for CNNs Inference on Board Satellites (2021)** | FPGA-accelerated CNNs for satellite imaging | Demonstrated higher efficiency of FPGA-based CNNs compared to Myriad 2 VPU | Validates FPGA’s advantages in onboard AI processing for autonomous satellite operations |
| **Resource-Constrained FPGA Design for Satellite Component Feature Extraction (2023)** | Optimizing FPGA design under resource constraints for space applications | Developed low-power FPGA architecture for satellite AI inference | Addresses trade-offs in FPGA power efficiency and computational performance |
| **Review on Hardware Devices and Software Techniques Enabling Neural Network Inference Onboard Satellites (2024)** | Comprehensive review of FPGA and ASIC implementations for AI onboard satellites | Analyzed trade-offs between ASICs and FPGAs for deep learning inference | Provides comparative insights into AI acceleration for space missions |
| **High-Performance Embedded Computing in Space: Evaluation of Processing Architectures for Vision-Based Navigation (2018)** | Comparison of different embedded processing architectures for vision-based navigation | FPGAs demonstrated superior energy efficiency over GPUs and CPUs in space | Supports FPGA’s suitability for low-power real-time navigation applications |
| **Trends and Patterns of ASIC and FPGA Use in European Space Missions (2012)** | Long-term study on the evolution of ASIC and FPGA use in European space projects | Shift from ASICs to FPGAs due to flexibility and cost efficiency | Shows historical trends in hardware selection for space applications |
| **FPGA vs. ASIC: A Comprehensive Comparison (2021)** | In-depth comparison of FPGA and ASIC performance, power, and cost | FPGAs excel in adaptability, ASICs in efficiency and power consumption | Key reference for trade-off analysis in satellite hardware selection |
| **ASIC vs FPGA: A Comparison of Hardware Solutions (2022)** | Comparison of ASIC and FPGA in different embedded systems | ASICs offer long-term reliability while FPGAs enable in-orbit reconfiguration | Highlights critical considerations for mission-specific hardware selection |
| **Development of a 32-channel ASIC for an X-ray APD Detector onboard the ISS (2017)** | ASIC-based sensor design for space-based X-ray detection | ASIC optimized for power efficiency and real-time radiation detection | Showcases ASIC’s advantage in specialized scientific instrumentation |
| **Review on Hardware Devices and Software Techniques Enabling Neural Network Inference Onboard Satellites (2023)** | Survey on AI inference accelerators for space applications | Discussed FPGA-based deep learning solutions and ASIC NPUs | Explores the evolving role of AI in space-based embedded systems |

**4. Key Themes and Analysis Embedded Satellite Systems: FPGA vs. ASIC**

**4.1 Radiation Tolerance and Reliability**

Radiation tolerance is one of the most critical considerations in space-based embedded systems. Electronic components in space are exposed to high levels of radiation, leading to potential single-event upsets (SEUs), total ionizing dose (TID) degradation, and latch-up effects. The choice between FPGAs and ASICs for space applications must account for their resilience to these hazards.

* ASICs offer inherent radiation hardness when designed with Radiation-Hardened By Design (RHBD) methodologies. These ASICs feature triple-well isolation, error correction mechanisms, and latch-up protection, ensuring high reliability in extreme environments.
* Radiation-Hardened FPGAs (e.g., Xilinx Virtex-5QV, Microsemi RTG4) are designed for space applications, though they lag behind commercial FPGAs in processing capability and efficiency.
* Commercial-Off-The-Shelf (COTS) FPGAs can be used in low Earth orbit (LEO) missions if proper shielding and redundancy techniques are applied.

**Case Studies:**

* Bensikaddour et al. implemented a chaos-based encryption scheme on an FPGA while integrating Triple Modular Redundancy (TMR) to counteract SEU vulnerabilities.
* Rapuano et al. evaluated Myriad 2-based AI accelerators vs. FPGA solutions for short-duration LEO missions, showing that COTS FPGAs, when shielded, can meet mission reliability standards.

**4.2 Performance and Power Efficiency**

The efficiency of space computing is dictated by performance-per-watt, as satellites operate under strict power constraints while handling high computational workloads such as AI inference, cryptography, and hyperspectral imaging.

* FPGAs provide high throughput due to fine-grained parallelism, making them ideal for real-time AI inference, image recognition, and signal processing.
* ASICs, when mass-produced, surpass FPGAs in energy efficiency, delivering higher processing power at lower power consumption for fixed-function tasks.
* FPGAs generally consume more power than ASICs, but their power consumption can be optimized with low-power architectures and dynamic scaling.

**Case Studies:**

* Rapuano et al. (CloudScout Mission) found that FPGA-based AI inference was 2.4× faster than Myriad 2 VPU but also had 1.8× higher power consumption.
* Lentaris et al. demonstrated that FPGAs achieved the best GFLOPS/W ratio among embedded CPUs, DSPs, and GPUs, proving superior for real-time spacecraft navigation.

**4.3 Reconfigurability and Upgradability**

For long-term satellite missions, hardware flexibility is a critical advantage. FPGAs enable post-launch reconfigurability, allowing for software-defined updates to AI models, encryption protocols, and onboard decision-making algorithms.

* FPGAs allow real-time adaptation, making them essential for autonomous satellites requiring AI evolution.
* ASICs remain fixed after fabrication, which limits their use in missions requiring continuous updates.
* Reconfigurable SoCs (e.g., Xilinx Zynq UltraScale+) combine FPGA fabric with embedded CPUs, allowing dynamic acceleration of specific AI tasks and cryptographic functions.

**Case Studies:**

* Guesmi et al. showcased partial FPGA reconfiguration for cryptographic security, allowing real-time encryption updates to mitigate evolving cybersecurity threats.
* NASA and ESA deep-space missions increasingly integrate FPGA-based AI accelerators, allowing for software-defined feature extraction, fault detection, and spacecraft autonomy.

**4.4 Development Cost, Complexity, and Time-to-Market**

The economic feasibility of satellite missions is influenced by development costs, design complexity, and time-to-market constraints.

* ASICs have high non-recurring engineering (NRE) costs due to custom fabrication processes, making them viable only for high-volume satellite constellations.
* FPGAs, despite having higher per-unit costs, reduce design risk and accelerate prototyping, making them ideal for small-scale or experimental missions.
* Time-to-market is a crucial factor, and FPGA-based systems can be rapidly deployed, while ASIC development cycles can extend mission timelines significantly.

**Case Studies:**

* Guesmi et al. used High-Level Synthesis (HLS) for FPGA-based AI cryptographic pipelines, reducing development complexity and time-to-deployment.
* Lentaris et al. observed that NASA and ESA space missions frequently rely on FPGAs for early-stage testing, as prototyping on FPGA platforms is significantly faster than developing an ASIC.

**4.5 Use Cases in Embedded Satellite Systems: AI, Image Processing, Cryptography**

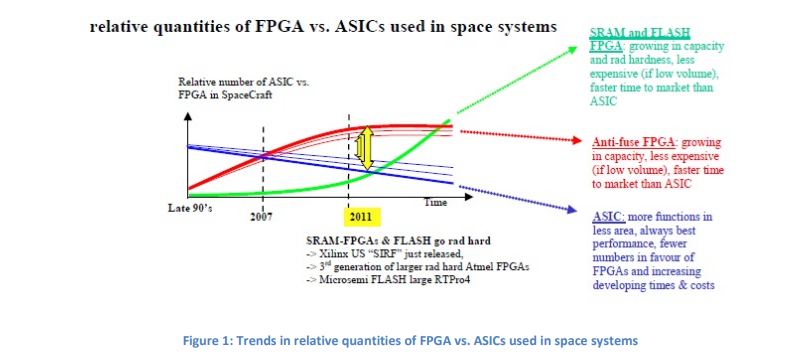
The increasing demand for autonomous space operations has led to a surge in AI-driven and security-focused applications, where FPGA and ASIC technologies play complementary roles.

* **AI Inference Acceleration:**
  + FPGAs dominate in AI-based navigation, object detection, and in-orbit analysis, offering programmability and adaptability.
  + ASIC-based Neural Processing Units (NPUs) are increasingly explored for power-efficient fixed AI models, though they lack post-launch flexibility.
* **Image Processing & Hyperspectral Imaging:**
  + FPGAs are widely used for onboard feature extraction and classification, enabling autonomous spacecraft decision-making.
  + ASICs could reduce power consumption for specific image processing algorithms, making them beneficial for long-duration missions with low computational variability.
* **Image Encryption & Cryptographic Security:**
  + Chaos-based encryption on FPGA (Bensikaddour et al., Guesmi et al.) ensures real-time security processing while integrating anti-SEU strategies.
  + ASIC-based cryptographic accelerators could reduce power consumption in highly secure, mass-produced satellite networks, though they cannot be updated post-deployment**.**

**Overall Analysis**

This analysis underscores the distinct advantages of FPGA and ASIC architectures in space computing:

* FPGAs excel in reconfigurable, AI-driven satellite applications, where real-time updates and high-throughput computing are required.
* ASICs dominate in fixed-function, low-power applications, particularly in long-duration deep-space missions requiring radiation tolerance and energy efficiency.
* A hybrid approach integrating FPGAs for adaptive AI processing and ASICs for fixed-function low-power tasks could provide the best balance between performance, flexibility, and efficiency in future satellite missions.
* **Analysis of Figure 1: Trends in Relative Quantities of FPGA vs. ASICs Used in Space Systems**

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This figure illustrates the evolving trend of FPGA and ASIC usage in space systems over time, highlighting the increasing adoption of FPGAs compared to ASICs. The graph provides insights into how different FPGA technologies (SRAM-based, Flash-based, and Anti-fuse) are gaining traction in satellite applications, while ASICs remain dominant in high-performance, fixed-function tasks.

* **Observations from the Figure**

1. **Shift from ASICs to FPGAs Over Time:**
   * In the late 1990s, ASICs were the dominant technology in space systems due to their performance and reliability.
   * By 2007, the trend began shifting towards FPGAs, driven by their increasing capacity, radiation tolerance, and flexibility.
   * By 2011, SRAM-based and Flash-based FPGAs had advanced significantly, further reducing the reliance on ASICs.
2. **Different FPGA Technologies and Their Growth:**

* **SRAM and Flash FPGAs (Green Line):**
  + - These are growing in capacity and radiation hardness.
    - They offer lower costs for small-volume production and faster time-to-market than ASICs.
    - Examples include Xilinx’s US “SRF” series, Atmel rad-hard FPGAs, and Microsemi Flash-based RT Pro4.
* **Anti-fuse FPGAs (Red Line):**
  + - These are also growing in capacity and adoption for space applications.
    - They are less expensive than ASICs for low-volume production and have a faster time-to-market.

1. **ASICs Remain in Niche High-Performance Applications (Blue Line):**
   * ASICs provide the best performance per watt and highest reliability in extreme space conditions.
   * However, their use is declining relative to FPGAs, primarily due to higher development costs and longer production timelines.
   * ASICs are still used for mission-critical, radiation-hardened applications that require absolute reliability.

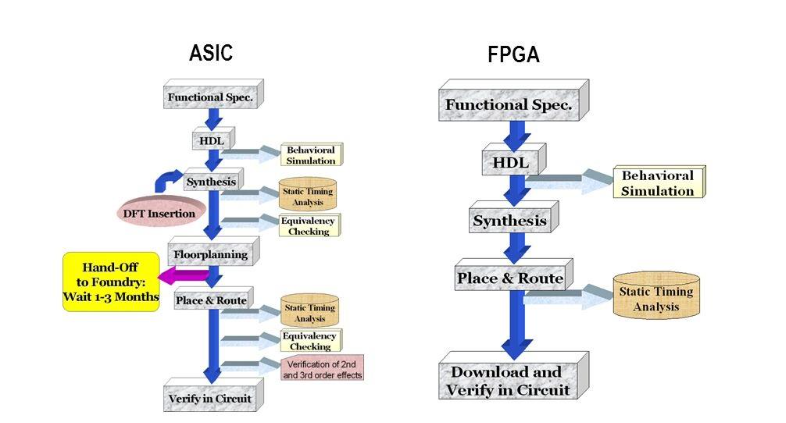
**6. Comprehensive Comparative Analysis of FPGA vs. ASIC in Satellite Embedded Systems**

| **Feature** | **FPGA** | **ASIC** |
| --- | --- | --- |
| **Design Flexibility** | High (Reconfigurable) | Low (Fixed Design) |
| **Power Efficiency** | Moderate | Optimized for Low Power |
| **Security** | Vulnerable to bitstream attacks | More secure (Hardwired Logic) |
| **Radiation Tolerance** | Susceptible to soft errors | Resistant to radiation effects |
| **Processing Speed** | High parallel processing | Optimized for fixed operations |
| **Development Cost** | Lower initial cost, reconfigurable | High upfront cost, low per-unit cost in large production |
| **Lifespan & Reliability** | Moderate, needs SEU protection | High, robust in extreme space conditions |
| **Application Suitability** | AI processing, real-time analysis, secure transmission | Long-term optimized processing, high-speed data handling |
| **Reconfigurability** | Can be updated in orbit | Fixed function, cannot be modified |
| **Manufacturing Complexity** | Easier to develop, shorter time-to-market | Requires complex fabrication and validation |

* **Advantages and Disadvantages of FPGA and ASIC in Space-Based Applications**

| **Criteria** | **FPGA Advantages** | **FPGA Disadvantages** | **ASIC Advantages** | **ASIC Disadvantages** |
| --- | --- | --- | --- | --- |
| **Power Consumption** | Moderate efficiency, good for real-time AI & encryption | Generally higher power use than ASICs | Exceptional efficiency for strict power budgets | No adaptability post-launch |
| **Reconfigurability** | Highly flexible, can be reprogrammed in orbit | Requires **bitstream security measures** | Fixed function, highly optimized | Cannot be updated after deployment |
| **Performance** | High parallel processing, ideal for **AI inference, cryptography** | **Lower efficiency per watt** than ASIC | Optimized for specific tasks, superior performance per watt | Fixed functionality limits AI upgrades |
| **Radiation Tolerance** | Can be hardened using **TMR and ECC techniques** | Requires additional mitigation measures | High radiation resistance | **Designing radiation-hardened ASICs increases complexity** |
| **Development Cycle** | **Shorter development cycles**, faster prototyping | Higher power consumption may impact energy budgets | High reliability and robustness, ideal for long-term missions | **Expensive and time-consuming to develop** |
| **Lifecycle & Cost** | Lower initial cost, good for experimental missions | Higher **long-term operational cost** due to power consumption | **Better long-term value for deep-space missions** | **Long ASIC development cycle increases time-to-market** |

* Figure 2. **Design Flow Comparison: ASIC vs. FPGA**



This figure provides a side-by-side comparison of the design flow for ASIC (Application-Specific Integrated Circuit) and FPGA (Field-Programmable Gate Array) implementations, highlighting the key differences in development time, complexity, and flexibility.

* **Observation**
* **ASIC Design Flow (Left Side)**
  + ASIC development follows a rigid and complex process, including Design for Testability (DFT) insertion, floorplanning, and physical verification.
  + After synthesis, the design undergoes floorplanning and place & route, followed by extensive verification steps to ensure correctness.
  + Hand-off to a foundry requires 1-3 months for fabrication, making the development cycle significantly longer.
  + ASICs require static timing analysis, equivalency checking, and verification of 2nd and 3rd order effects, adding more complexity before production.
  + Once manufactured, ASICs cannot be modified, meaning errors require a costly re-spin.
* **FPGA Design Flow (Right Side)**
  + FPGA development is faster and more flexible, as it does not require physical fabrication.
  + After synthesis and place & route, the design is immediately tested in hardware, avoiding the long wait times seen in ASIC manufacturing.
  + Behavioral simulation and static timing analysis are still required, but verification is done in a reprogrammable environment.
  + Unlike ASICs, FPGAs allow real-time reconfiguration and updates, making them ideal for prototyping and iterative development.
* **Similarities and Differences Between FPGA and ASIC in Satellite Embedded Systems**

| **Aspect** | **Similarities** | **Differences** |
| --- | --- | --- |
| **Application** | Both are used in satellite computing | FPGA is reconfigurable, ASIC is fixed post-launch |
| **Radiation Tolerance** | Both can be radiation-hardened | FPGA requires TMR/ECC, ASICs have inherent robustness |
| **Processing Capability** | Both handle intensive space computations | FPGA is parallel-processing, ASIC is fixed-function optimized |
| **Reliability** | Both can be engineered for high reliability | FPGA needs radiation protection, ASIC has built-in reliability |
| **Development Considerations** | Both require extensive space testing | FPGA has faster prototyping, ASIC has longer production cycles |
| **Power Management** | Both optimize power for space missions | FPGA has higher power consumption, ASIC is more efficient |

* **Key Takeaways and Future Considerations**

1. **FPGA vs. ASIC Trade-offs in Space:**
   * FPGAs provide unmatched adaptability, reconfigurability, and rapid prototyping, making them ideal for AI-driven satellites, secure communications, and real-time reconfigurable computing.
   * ASICs provide superior power efficiency, processing speed, and radiation tolerance, making them more suitable for long-term deep-space missions where adaptability is not required.
2. **Hybrid FPGA-ASIC Architectures for Next-Generation Satellites:**
   * Future satellite designs may combine FPGA flexibility with ASIC efficiency, creating hybrid architectures that enable in-orbit AI upgrades while maintaining low power operation for mission-critical tasks.
3. **Advancements in Radiation-Hardened FPGA & AI Processors:**
   * New space-grade FPGA architectures (e.g., Microsemi RTG4, Xilinx Versal AI Edge) are being developed to bridge the performance-power gap between traditional FPGAs and ASICs.
   * ASIC-based NPUs (Neural Processing Units) could enable low-power, high-speed AI inference for fully autonomous spacecraft.
4. **Evolving Use Cases in Space AI & Secure Communications:**
   * AI-powered Earth observation satellites require continuous CNN updates, making FPGAs a dominant choice.
   * High-security, encrypted satellite transmissions benefit from ASIC-based cryptographic engines, ensuring low power, high-speed encryption.

**6.1. Circuit Hardware Design for FPGA and ASIC in Satellites**

**6.1.1 FPGA-Based Solutions**

Field Programmable Gate Arrays (FPGAs) have increasingly become integral to satellite embedded systems, driven primarily by their inherent flexibility and reconfigurability. Key attributes include:

* **High Reconfigurability:** FPGAs offer unmatched flexibility through their ability to be reprogrammed post-launch, allowing dynamic updates to algorithms and mission objectives. This reconfigurability is crucial for adaptive missions, experimental payloads, and AI-based satellite applications requiring in-orbit learning and adjustments.
* **Moderate Power Efficiency:** While FPGA implementations typically have moderate power efficiency compared to ASICs, advancements such as model quantization and custom caching strategies significantly improve their energy profile. Despite this, their power consumption remains higher relative to ASICs for dedicated, unchanging tasks.
* **Security Considerations:** FPGA-based systems are vulnerable to bitstream extraction or tampering attacks, highlighting a need for secure bitstream storage and encryption techniques when used in sensitive satellite missions.
* **Radiation Tolerance:** FPGAs, particularly SRAM-based, are susceptible to radiation-induced soft errors (Single Event Upsets). Radiation mitigation typically involves redundancy strategies (e.g., Triple Modular Redundancy—TMR) or scrubbing techniques to maintain integrity, though these methods incur additional overhead.
* **Processing Speed and Parallelism:** FPGAs excel at parallel processing, offering significant speed-ups for real-time AI inference, image processing, and cryptographic tasks. Their ability to run operations concurrently significantly reduces latency, crucial for autonomous satellite navigation and immediate onboard data analysis.
* **Manufacturing Complexity and Cost:** FPGA development is comparatively simpler and involves shorter design cycles, lower upfront costs, and faster time-to-market. This makes them advantageous for experimental or smaller-scale missions.

**6.1.2 FPGA-Based Embedded System Architecture:**

* **FPGA-Based Embedded System Architecture for Satellite Applications**

FPGA-based architectures offer high adaptability, real-time processing efficiency, and in-orbit reconfigurability, making them ideal for satellite embedded systems. Below is a breakdown of key architectural components that optimize FPGA performance in space missions:

**1. Soft Processors (e.g., MicroBlaze, Nios II)**

* Provide embedded computing flexibility for real-time control and data processing tasks.
* MicroBlaze (Xilinx) and Nios II (Intel) are widely used soft processors integrated within FPGA fabric.
* Trade-off: They offer flexibility but have lower computational power than dedicated processors.
* Use Cases: Ideal for mission control tasks, sensor data handling, and protocol management.

**2. DSP Blocks for Real-Time AI & Signal Processing**

* FPGAs integrate dedicated DSP slices, which enable efficient digital signal operations.
* Critical for:
  + Hyperspectral image processing
  + AI inference acceleration (e.g., CNN-based onboard processing)
  + High-speed modulation/demodulation for satellite communications
* Advantage: Provides low-latency, high-speed processing without external DSP chips.

**3. Configurable Custom Caches & Memory Management**

* Optimized caching mechanisms enhance data throughput and minimize processing latency.
* On-chip RAM & LUT-based cache optimizations improve access times for:
  + AI models running onboard satellites
  + Cryptographic data processing
  + Streaming real-time satellite imagery
* Hybrid Memory Architectures: Some FPGA designs integrate external DDR memory with on-chip cache for faster data retrieval.

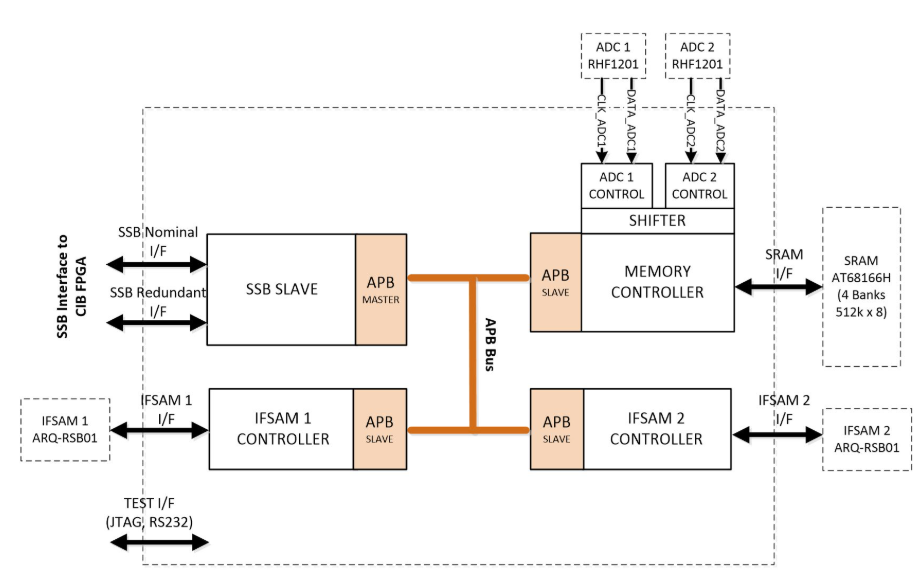
**4. High-Speed I/O Interfaces for Real-Time Data Exchange**

* Gigabit Ethernet, SpaceWire, PCIe, and custom LVDS channels allow rapid onboard communication.
* Key for:
  + High-bandwidth satellite telemetry processing
  + High-resolution sensor data transmission
  + AI-accelerated onboard decision-making systems
* Integration with external ASIC accelerators further enhances data throughput efficiency.

**5. Reconfiguration Modules for In-Orbit Updates & Adaptability**

* Partial and dynamic FPGA reconfiguration enables real-time hardware updates without requiring new satellite deployments.
* Key for:
  + AI model updates for object detection in space
  + Software-defined radio (SDR) frequency adjustments
  + Adaptive cryptographic security enhancements
* Advantages:
  + Mission longevity—hardware can evolve post-launch.
  + Fault-tolerant systems—adaptive reconfiguration mitigates SEU-induced failures.

***Figure 4:*** *FPGA-Based Satellite Interface System*



This diagram represents an FPGA-based satellite interface system, utilizing APB (Advanced Peripheral Bus) communication for data transfer between memory, controllers, and sensors.

**Observation:**

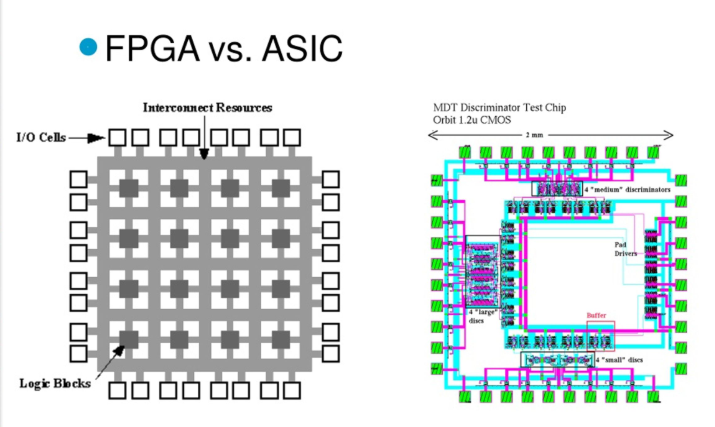
* **SSB Interface:** Connects the FPGA to redundant and nominal data channels, ensuring reliability.
* **APB Bus:** Acts as the central communication backbone, linking controllers and memory components.
* **Memory Controller:** Manages SRAM storage and ADC (Analog-to-Digital Converter) inputs for signal processing.
* **IFSAM Controllers:** Handle interfacing and communication protocols, ensuring synchronized data processing.
* **Test Interface (JTAG, RS232):** Allows system testing and debugging.
* **Summary:**

This FPGA-driven architecture ensures real-time data acquisition and processing for satellite applications, integrating redundant safety measures, efficient memory access, and high-speed communication interfaces. The system’s modularity and reliability make it ideal for mission-critical operations in space environments.

**6.1.2 ASIC-Based Solutions**

Application-Specific Integrated Circuits (ASICs) are tailored explicitly for mission-specific functionalities, delivering significant performance, power efficiency, and reliability advantages for long-duration, high-reliability satellite applications. Key characteristics include:

* **Optimized Power Efficiency:** ASICs are designed for minimal power consumption, making them ideal for deep-space missions or prolonged missions where energy conservation is paramount.
* **Enhanced Security:** Hardwired logic in ASICs inherently provides greater resistance against hardware-level attacks compared to FPGAs, due to their fixed functionality post-manufacturing.
* **Superior Radiation Hardening:** ASICs leverage advanced radiation-hardening techniques, ensuring robust performance against single-event upsets (SEUs) and other radiation-induced errors, crucial for reliable long-term space operations.
* **High Processing Performance:** ASICs offer optimized speed and efficiency for specific, repetitive tasks such as sensor data handling, communication modulation, and dedicated neural network inference, outperforming FPGAs in terms of throughput for these fixed operations.
* **Manufacturing and Cost Implications:** ASIC development entails substantial upfront investment, complex fabrication processes, rigorous testing, and validation. While initial costs are high, per-unit costs become advantageous for high-volume production or long-term missions.
* **Limited Flexibility:** ASICs’ fixed logic cannot be altered post-manufacturing, limiting in-orbit adaptability and updates, a critical consideration for evolving mission objectives.
* **ASIC-Based Embedded System Architecture:**
* **Fixed Logic Processors:** Highly optimized for efficiency, suited for predefined mission-critical tasks.
* **Radiation-Hardened Memory (SRAM, DRAM):** Ensures reliability and integrity of stored data in radiation-rich environments.
* **Custom Analog and Digital Signal Processing Units:** Specialized for efficient onboard data processing and communication.
* **Secure Design:** Built-in security features through hardwired logic, protecting against tampering and cyber threats.
* **Figure 3 FPGA vs. ASIC Architecture**

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**Analysis of FPGA vs. ASIC Architecture**

This figure visually compares FPGA and ASIC architectures, highlighting their structural differences and design methodologies.

* **Left Side (FPGA Architecture)**
  + The diagram represents an FPGA structure, showing logic blocks, interconnect resources, and I/O cells.
  + Logic Blocks: These are reprogrammable units that perform computational tasks.
  + Interconnect Resources: These enable programmable connections between logic blocks, allowing flexible design implementation.
  + I/O Cells: Positioned on the periphery, they provide connectivity to external devices.
  + Key Advantage: FPGAs offer high flexibility and adaptability, making them ideal for prototyping, AI acceleration, and reconfigurable computing in space systems.
* **Right Side (ASIC Architecture)**
  + This is a custom ASIC layout, designed for specific tasks with fixed logic and optimized performance.
  + The labeled sections indicate specialized functions like discriminators, buffers, and pad drivers, showing a tailored circuit design optimized for efficiency and reliability.
  + Unlike FPGAs, ASICs do not have programmable interconnects, meaning they provide higher performance and lower power consumption but lack flexibility.
  + Key Advantage: ASICs are highly efficient and reliable, making them suitable for long-duration, radiation-hardened space applications where adaptability is not required.
* **Relevance to Satellite Embedded Systems**
* **Mission Profile Considerations:** ASICs excel in missions with stable, predictable tasks due to their power efficiency and reliability, while FPGAs are essential for missions requiring adaptive, flexible capabilities and updates post-launch.
* **Hybrid Architectures:** Future satellite missions may increasingly leverage hybrid FPGA-ASIC architectures, harnessing the adaptability and parallel processing strengths of FPGAs with ASICs’ superior power efficiency, radiation resilience, and security, delivering optimized satellite embedded computing solutions.

## **7. Conclusion**

The comparative analysis of FPGAs and ASICs in satellite embedded systems highlights the critical trade-offs between reconfigurability, power efficiency, processing speed, and radiation tolerance. FPGAs are increasingly favored for AI-driven, real-time applications, enabling on-orbit reconfiguration and adaptability, making them ideal for short-term missions, evolving AI models, and secure communications. Conversely, ASICs remain the gold standard for power-efficient, high-reliability, and radiation-hardened space applications, particularly for deep-space, long-duration missions where flexibility is not required.

**Key Takeaways from the Literature Review:**

* FPGAs offer shorter development cycles, adaptability, and high parallel processing, making them ideal for AI inference, cryptography, and real-time data processing in space.
* ASICs provide superior power efficiency and computational optimization, ensuring low power consumption and high reliability for fixed-function satellite applications.
* Hybrid FPGA-ASIC architectures may combine the reconfigurability of FPGAs with the efficiency of ASICs, optimizing both computational adaptability and energy efficiency in future satellite missions.
* **Future Research Directions**

1. **Developing Standardized Benchmarks**
   * There is currently no universal benchmark for comparing FPGA and ASIC performance in space computing.
   * Future studies should focus on defining metrics such as GFLOPS/Watt, power-to-performance ratio, and radiation tolerance reliability.
2. **Enhancing In-Orbit Partial Reconfiguration**
   * While FPGA reconfiguration is often cited as a key advantage, practical space implementations remain limited.
   * Further research is required to enable AI model updates and cryptographic protocol enhancements during missions.
3. **Radiation-Resilient AI Acceleration**
   * The adoption of radiation-hardened FPGAs and low-power ASIC-based neural processing units (NPUs) should be explored to enhance autonomous onboard AI capabilities.
4. **Hybrid FPGA-ASIC Architectures for Next-Generation Satellites**
   * Future satellite designs may benefit from hybrid processing architectures, where FPGAs handle real-time AI inference while ASICs ensure energy-efficient, mission-critical computing.

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